Agora 2.0 Migration

Pin Assignment Updates

Application Note

Embedded Planet Inc. | v1.1.0 | 14 JUL 2025

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1. ABOUT THIS APPLICATION NOTE

The Agora module has undergone a hardware update and upgrade. With the end of life of the Telit ME910C1, the replacement ME910G1 required some hardware modifications. Additional changes were made to remove unused features and add often requested features (like an onboard tricolor LED and expanded GPIO for custom use). This new Agora module is identified as Agora 2.0 and a number of connections to the processor (BT840/nRF52840) are required.

The following note describes the firmware updates required to support the upgrade.

2. PIN ASSIGNMENTS

Specific pin assignments have changed to support the ME910G1, tricolor LED, and GPIO access.

2.1. CELL PIN ASSIGNMENTS

The following pin assignments differ between the base Agora module and the Agora 2.0 module:

PIN DEFINITION	AGORA PIN ASSIGNMENT	AGORA 2.0 PIN ASSIGNMENT
CELL_PWR_EN	NRF_GPIO_PIN_MAP(0,28)	NRF_GPIO_PIN_MAP(0,04)
CELL_ON_OFF	NRF_GPIO_PIN_MAP(0,30)	NRF_GPIO_PIN_MAP(0,19)
CELL_TX_PIN_NUMBER	NRF_GPIO_PIN_MAP(1,02)	NRF_GPIO_PIN_MAP(1,12)
CELL_DSR_PIN_NUMBER	NRF_GPIO_PIN_MAP(1,03)	NRF_GPIO_PIN_MAP(1,13)
CELL_DTR_PIN_NUMBER	NRF_GPIO_PIN_MAP(1,04)	NRF_GPIO_PIN_MAP(1,14)
CELL_RTS_PIN_NUMBER	NRF_GPIO_PIN_MAP(0,14)	NRF_GPIO_PIN_MAP(0,11)

Hardware flow control for cell communication is seldomly if ever used. The hardware control pins have been repurposed to be used as GPIO. If hardware flow is required for your design requirements, the flow control can be restored with the following hardware updates (contact Embedded Planet for specific hardware needs):

- Cell DCD has been repurposed to GPIO9, to use cell DCD, populate R26 (0 Ohm).
- Cell DSR has been repurposed to GPIO7, to use cell DSR, populate R25 (0 Ohm).
- Cell DTR has been repurposed to GPIO8, to use cell DTR, populate R27 (0 Ohm).

2.2. QSPI PIN ASSIGNMENTS

The following pin assignments differ between the base Agora module and the Agora 2.0 module, with the QSPI signals removed from the edge connector and now routed only between the processor and onboard QSPI:

PIN DEFINITION	AGORA PIN ASSIGNMENT	AGORA 2.0 PIN ASSIGNMENT
BSP_QSPI_CSN_PIN	NRF_GPIO_PIN_MAP(0,17)	NRF_GPIO_PIN_MAP(1,09)
BSP_QSPI_SCK_PIN	NRF_GPIO_PIN_MAP(0,19)	NRF_GPIO_PIN_MAP(0,30)
BSP_QSPI_IO0_PIN	NRF_GPIO_PIN_MAP(0,20)	NRF_GPIO_PIN_MAP(1,03)
BSP_QSPI_IO1_PIN	NRF_GPIO_PIN_MAP(0,21)	NRF_GPIO_PIN_MAP(0,31)
BSP_QSPI_IO2_PIN	NRF_GPIO_PIN_MAP(0,22)	NRF_GPIO_PIN_MAP(0,06)
BSP_QSPI_IO3_PIN	NRF_GPIO_PIN_MAP(0,23)	NRF_GPIO_PIN_MAP(0,05)

Note that the QSPI has a maximum data speed limited to 16MHz (QSPI_CONFIG_FREQUENCY is 1 of more).

2.3. LORA PIN ASSIGNMENTS

The following pin assignments differ between the base Agora module and the Agora 2.0 module:

PIN DEFINITION	AGORA PIN ASSIGNMENT	AGORA 2.0 PIN ASSIGNMENT
PIN_NAME_LORA_NSS	NRF_GPIO_PIN_MAP(1,09)	NRF_GPIO_PIN_MAP(1,04)
PIN_NAME_LORA_DIO1	NRF_GPIO_PIN_MAP(1,12)	NRF_GPIO_PIN_MAP(1,02)

LoRa DIO1 through DIO3 are seldomly if ever used and have been repurposed to be used as GPIO. If these signals are required for your design requirements, they can be restored with the following hardware updates (contact Embedded Planet for specific hardware needs):

- LoRa_DIO1 has been repurposed to GPIO6, to use LoRa_DIO1, populate R28 (0 Ohm).
- LoRa_DIO2 has been repurposed to GPIO7, to use LoRa_DIO2, populate R29 (0 Ohm).
- LoRa_DIO3 has been repurposed to GPIO8, to use LoRa_DIO3, populate R20 (0 Ohm).

2.4. SENSOR AND GPIO PIN ASSIGNMENTS

The following pin assignments differ between the base Agora module and the Agora 2.0 module:

PIN DEFINITION	AGORA PIN ASSIGNMENT	AGORA 2.0 PIN ASSIGNMENT
PIN_NAME_INT_TOF	NRF_GPIO_PIN_MAP(0,04)	NRF_GPIO_PIN_MAP(0,28)
BAT_MON_EN_PIN	NRF_GPIO_PIN_MAP(1,11)	NRF_GPIO_PIN_MAP(0,14)
PIN_NAME_SENSOR_POWER_ENABLE	NRF_GPIO_PIN_MAP(0,31)	NRF_GPIO_PIN_MAP(0,20)
PIN_NAME_I2S_SCK	NRF_GPIO_PIN_MAP(0,06)	NRF_GPIO_PIN_MAP(0,17)
PIN_NAME_TE_GPIO1	NRF_GPIO_PIN_MAP(0,30)	NRF_GPIO_PIN_MAP(0,19)
PIN_NAME_TE_GPIO5	NRF_GPIO_PIN_MAP(0,06)	NRF_GPIO_PIN_MAP(0,17)

Additional pins are now available on the edge connector:

PIN DEFINITION	AGORA PIN ASSIGNMENT	AGORA 2.0 PIN ASSIGNMENT
PIN_NAME_TE_GPIO6	-	NRF_GPIO_PIN_MAP(1, 2)
PIN_NAME_TE_GPIO7	-	NRF_GPIO_PIN_MAP(1,13)
PIN_NAME_TE_GPIO8	-	NRF_GPIO_PIN_MAP(1,14)
PIN_NAME_TE_GPIO9	-	NRF_GPIO_PIN_MAP(0,15)

The edge connections assignments correspond to the following locations on the edge connector:

- PIN_NAME_TE_GPIO1 – TE1 Pin B9
- PIN_NAME_TE_GPIO2 – TE1 Pin B10, Pin assignment remains: NRF_GPIO_PIN_MAP(0,31)
- PIN_NAME_TE_GPIO3 – TE1 Pin B11, Pin assignment remains: NRF_GPIO_PIN_MAP(0,26)
- PIN_NAME_TE_GPIO4 – TE1 Pin A6, Pin assignment remains: NRF_GPIO_PIN_MAP(0,08)
- PIN_NAME_TE_GPIO5 – TE1 Pin A7
- PIN_NAME_TE_GPIO6 – TE1 Pin B15
- PIN_NAME_TE_GPIO7 – TE1 Pin B16
- PIN_NAME_TE_GPIO8 – TE1 Pin B17
- PIN_NAME_TE_GPIO9 – TE1 Pin B18

2.5. LED PIN ASSIGNMENTS

The following pin assignments differ between the base Agora module and the Agora 2.0 module, the RED led is typically defined as “LED_1”:

PIN DEFINITION	AGORA PIN ASSIGNMENT	AGORA 2.0 PIN ASSIGNMENT
LED_1	NRF_GPIO_PIN_MAP(0,05)	NRF_GPIO_PIN_MAP(0,22)

The LED now supports Green (LED_2) and Blue (LED_3):

PIN DEFINITION	AGORA PIN ASSIGNMENT	AGORA 2.0 PIN ASSIGNMENT
LED_2	-	NRF_GPIO_PIN_MAP(0,23)
LED_3	-	NRF_GPIO_PIN_MAP(0,21)

The LEDs on Agora 2.0 are now active high, in the Agora product the red LED is active low.

2.6. I/O VOLTAGE

The Agora 2.0 has a different power configuration than the original Agora module allowing the Agora 2.0 to have lower operating and idle currents. With the updated power scheme the I/O voltage must be configured, without it the Agora 2.0 will default to an I/O voltage of 1.8V.

The following code can be used as part of the system initialization. The code checks to see if the I/O voltage is set to 3.3V and updates the device if not properly set (the device will reboot after the voltage is set). The system voltage setting is held in non-volatile memory, so the I/O voltage is updated on the first boot up of the device and will remain at 3.3V thereafter.

```
if ((NRF_UICR->REGOUT0 & UICR_REGOUT0_VOUT_Msk) !=
    (UICR_REGOUT0_VOUT_3V3 << UICR_REGOUT0_VOUT_Pos))
{

   NRF_NVMC->CONFIG = NVMC_CONFIG_WEN_Wen << NVMC_CONFIG_WEN_Pos;
   while (NRF_NVMC->READY == NVMC_READY_READY_Busy){}
   NRF_UICR->REGOUT0 = (NRF_UICR->REGOUT0 &
                        ~((uint32_t)UICR_REGOUT0_VOUT_Msk)) |
                        (UICR_REGOUT0_VOUT_3V3 << UICR_REGOUT0_VOUT_Pos);

   NRF_NVMC->CONFIG = NVMC_CONFIG_WEN_Ren << NVMC_CONFIG_WEN_Pos;
   while (NRF_NVMC->READY == NVMC_READY_READY_Busy){}

   /* a reset is required for changes to take effect */
   NVIC_SystemReset();
}
```

3. DOCUMENT HISTORY

Revision	Author	Description	Date
1.0.0	M. Timieski	Initial Release	03 MAR 2025
1.1.0	M. Timieski	QSPI Maximum update	14 JUL 2025

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